R E M A R K S

Reconsideration of this application is respectfully requested.

Claims 1-16 were again rejected under 35 USC 102 as being anticipated by USP 6,734,636 ("Sanford et al"). This rejection, however, is again respectfully traversed.

According to the present invention as recited in independent claim 1, a display apparatus is provided which comprises a plurality of pixel circuits, a plurality of light-emitting elements each of which is arranged for a corresponding one of the pixel circuits and emits light at a luminance corresponding to a driving current; luminance gray level designation means; and current value switching voltage output means.

In addition, according to claim 1, the luminance level display means is provided for supplying through a signal line to a respective one of the pixel circuits, a gray level designation current having a current value larger than that of the driving current during a selection period to store a luminance gray level of the light-emitting element in the pixel circuit.

Still further, according to claim 1, the current value switching voltage output means is provided for outputting a first voltage to the pixel circuit to cause the luminance gray level designation means to supply the gray level designation current through the signal line to the pixel circuit during the selection

period, and for outputting a second voltage having a potential different from that of the first voltage to the pixel circuit during a nonselection period, thereby modulating a current output from the pixel circuit based on the luminance gray level stored in the pixel circuit to supply the driving current to the pixel circuit.

According to independent claim 11, moreover, a driving method is provided for a display apparatus which comprises a plurality of pixel circuits and causes light-emitting elements each of which is arranged for a corresponding one of the pixel circuits to emit light in accordance with a predetermined driving current to execute display.

The method recited in claim 11 comprises: (i) outputting a first voltage to a respective one of the pixel circuits to supply a gray level designation current having a current value larger than that of the driving current through a signal line to the pixel circuit during a selection period and store, in the pixel circuit, a luminance gray level of the light-emitting element corresponding to the current value of the gray level designation current; and (ii) outputting a second voltage having a potential different from that of the first voltage to the pixel circuit during a nonselection period to modulate the driving current output from the pixel circuit based on the luminance gray level stored in the pixel circuit.

With the structure recited in independent claim 1, for example, in a selection period (for example, the selection period T_{SE} of an ith row in Fig. 5), current value switching voltage output means (for example, the power supply scanning driver 6) outputs a first voltage (for example, potential V_{HIGH}) to a plurality of pixel circuits (for example, pixel circuits $D_{i,1}$ to $D_{i,n}$) to cause luminance gray level designation means (for example, a data driver 3 in Fig. 1) to flow a gray level designation current. On the other hand, in a nonselection period (for example, nonselection period T_{NSE} in Fig. 5), the current value switching voltage output means outputs a second voltage (for example, potential V_{LOW}) to the plurality of pixel circuits, thereby flowing a driving current to the pixel circuits.

As shown in Fig. 5, the voltage of potential V_{HIGH} is higher than that of potential V_{LOW}. Moreover, as shown in Fig. 3, the pixel circuits comprise transistors 21, 22, and 23, and each transistor includes a gate, a source, and a drain. The current value of the current flowing between the drain and the source depends on the voltage between the drain and the source, and the voltage between the gate and the source.

Fig. 4 shows a general voltage-to-current characteristic of an n-channel transistor. The current value I_{DS} of a current flowing between the drain and the source of the transistor becomes greater as the voltage V_{GS} between the gate and the

source increases, when the voltage V_{DS} between the drain and the source is constant. Moreover, when the value of the voltage V_{GS} between the gate and the source is made constant, there is a tendency for the voltage V_{DS} between the drain and the source to become relatively great in a saturation region (at a high voltage) to become relatively small in a nonsaturation region (at a low voltage).

As explained in specification at page 29, line 25, to page 30, line 14, a gray level designation current, which is a saturation current (a current in the saturation region), is supplied to the transistor 23 by the first voltage, and in the nonselection period, the voltage V_{DS} of the transistor 23 is set in the nonsaturation region by the second voltage. Accordingly, the driving current flowing through the transistor 23 in the nonselection period becomes smaller than the gray level designation current flowing through the transistor 23 in the selection period.

Accordingly, with the structure of the present invention, by supplying a gray level designation current, which has a greater current value than the driving current, in advance, it is possible to avoid the undesired event that storing of an electric charge is delayed by parasitic capacitance. Accordingly, in the present invention, the voltage applied to the pixel circuits (in particular, between the source and the drain of a transistor) is

set to be large in a selection period and small in a nonselection period.

By contrast, Sanford et al discloses (column 7, lines 1-20) increasing a data line current and reducing the viewing time of the pixel data. That is, in a viewing state, if the data line current is further increased, the redundant current flows through a transistor Q202, and Q303, which brings about the advantage of being able to store the electric charge promptly in Cs210, and Cs310. However, since the charge stored in Cs210, and Cs310 becomes redundant, a current having a greater current value than desired in a high brightness gradation, in particular, will be supplied, and the display of the data will be brighter than necessary.

In order to avoid this problem, the viewing time of the data is reduced according to Sanford et al. More specifically, brightness per unit of time (which is dependent on the current value of a light-emitting element per unit of time) multiplied by the light emitting time (viewing time) is equal to apparent brightness. In Sanford et al, in order to maintain the apparent brightness, the increased amount of brightness per unit of time due to the flowing of the redundant current is suppressed by reducing the viewing time. In other words, in any event, in both of FIGS. 2 and 3 of Sanford et al, reducing the time of a viewing state supports the fact that the current in the viewing state is

a redundant current. Thus, it is obvious that the redundant current in the viewing state causes the redundant current in a writing state.

In view of the foregoing, it is respectfully pointed out that according to Sanford et al, the currents in the writing state and the viewing state are both redundant currents. Sanford et al does not indicate that the current in the viewing state is reduced as compared to the current in the writing state, as recited in claim 1.

As explained above, according to the present invention as recited in independent claims 1 and 11, the light emitting time is not changed according to the brightness per unit of time. By contrast, the (first) voltage applied to the pixel circuits (in particular, between the source and the drain of the transistor) is increased in a selection period (writing state). Accordingly, it is possible to increase the current per unit of time in a selection period, and rapidly store the electric charge. Furthermore, since the (second) voltage is reduced in a nonselection period (viewing state), the current per unit of time in the nonselection period is reduced, as compared to the current per unit of time in the selection period. Accordingly, it is possible to maintain the repeatability of the gradation. Thus, the present invention does not adjust the time of the viewing

state according to the current per unit of time, as performed in Sandford at al.

In Fig. 2 thereof, Sandford et al shows that the potential is increased to a higher level, i.e., at Vdd2, when transferring from the writing state to the viewing state. Here, since the voltage in the writing state (Vddl-Vss) is applied to the OLED 220 and the transistor Q203, and the voltage in the viewing state (Vdd2-Vss) (> (Vddl-Vss)) is also applied (to the OLED 220 and the transistor Q203), the voltage in the viewing state is higher than the voltage in the writing state. On the other hand, in FIG. 3, when transferring from the writing state to the viewing state, the potential is changed to a lower level, i.e., at Vssl. In such a state, the voltage in the writing state (Vdd-Vss2) is applied to the OLED 320 and the transistor Q303, which becomes the voltage in the viewing state (Vdd-Vssl) (>(Vdd-Vss2)). That is, the voltage in the viewing state is higher than the voltage in the writing state.

It is respectfully submitted that either case (Fig. 2 or Fig. 3) of Sanford et al is the same except for the point that the element which causes a voltage displacement is of a higher potential or of a lower potential. In Fig. 3, even if the potential is changed to a low potential (Vssl) in the viewing state, the current in the viewing state is not reduced, as in the present invention.

In view of the foregoing, it is respectfully submitted that Sanford et al does not disclose, teach or suggest the structure and method recited in independent claims 1 and 11.

Accordingly, it is respectfully submitted that the present independent claims 1 and 11, and claims 2-10 and 12-16 respectively depending therefrom, clearly patentably distinguish over Sanford et al under 35 USC 102 as well as under 35 USC 103

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Entry of this Amendment, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,

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